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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shunpei Yamazaki et al.                      Art Unit : 2822  
Serial No. : 10/730,047                                      Examiner : Roy Karl Potter  
Filed : December 9, 2003  
Title : SEMICONDUCTOR CHIP AND METHOD FOR MANUFACTURING THE  
SAME

**Mail Stop Amendment**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

REPLY TO ACTION OF JULY 13, 2005

Claims 1-26 are pending in the application with claims 1, 8, 15 and 23 being independent.

Initially, applicant acknowledges with appreciation the Examiner's allowance of claims 8-22, and the Examiner's indication that claims 2-5 and 7 are directed to allowable subject matter.

Claims 1 and 6 have been rejected as being anticipated by Bellaar (U.S. Patent No. 5,861,666). Applicant requests reconsideration and withdrawal of this rejection because Bellaar does not describe or suggest first and second device formative layers having thicknesses of at most 50  $\mu\text{m}$ . Applicant recognizes that, as set forth in the rejection, Bellaar, at col. 5, line 27-43, notes that an assembly of four chips is 1.2 mm high. However, applicant notes that 1.2 mm equals 1200  $\mu\text{m}$  and, even assuming for sake of argument that the layers of Bellaar's chips constitute formative layers, the 1200  $\mu\text{m}$  dimension of the assembly would in no way require thicknesses of those layers to be at most 50  $\mu\text{m}$ , as recited in claim 1.

Applicant submits that all claims are in condition for allowance.

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Attorney's Docket No.: 12732-185001 / US6821

A check in the amount of \$180.00 to cover the Information Disclosure Statement fee is enclosed. In the event that any additional fees are due, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 10/12/05

  
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